Incorporating Multicore Programming in Bachelor of Science in Computer Engineering Program

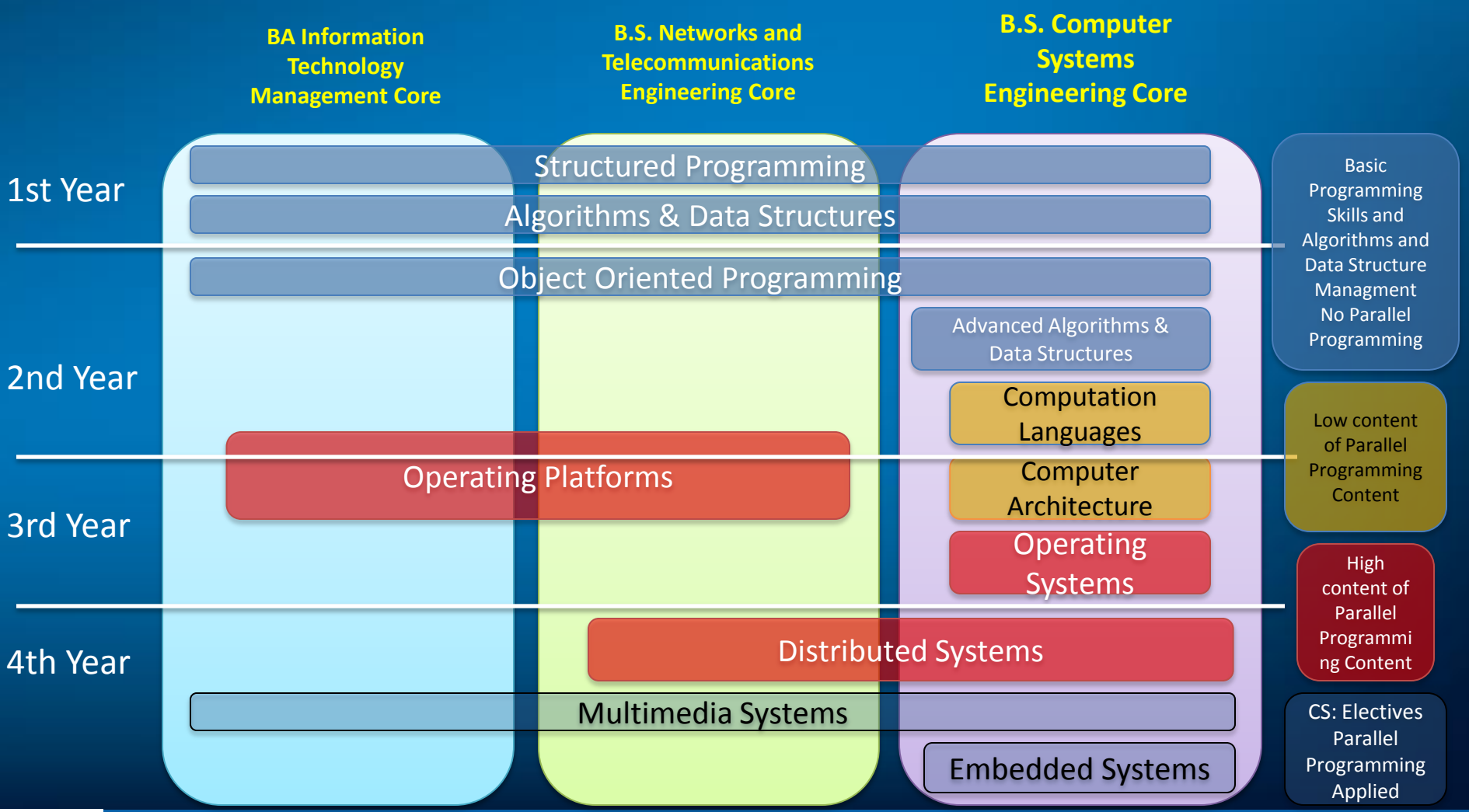
ITESO University
Guadalajara, Jalisco
México

Instituto Tecnológico y de Estudios Superiores de Occidente Jesuit University in Guadalajara

Population

- **Students: 8766**
  - **43.93 % Women**
  - **56.07 % Men**
- **From that population**
  - 74 Students in Networks and Communication engineering
  - 250 Students in Computer Systems engineering
  - 58 Students in major of Information Technology
  - 146 Students in Electronic engineering
  - 45 Students in Applied Informatics master degree
  - 90 Students in Electronic Design master degree
  - 7 Students in Integrated Circuits Design specialty
- **Professors: 312 staff + 990 course teachers**
  - Researchers (Staff): 77
  - SNI Researchers (Staff): 22
- **1 Campus in the Institute system:**

Parallel Programming in ITESO – Bachelors Curriculum



Operating Platforms

- Outline
  - CPU Architecture
  - Assembly Language
  - Multicore Architecture
    - Hyper Threading and Multicore
  - OS Processes
  - Threads
    - Multicore Software Impact
    - Tasks & Threads (Win Threads)
    - Threads Synchronization
      - Data Races and Deadlocks
    - Using tolls for performance & correctness
  - Memory Management
  - I/O Management

*Knowledge**

24 hrs

*Apply**

24 hrs

40 hrs/128 hrs = 37.5%

Total 128 hrs

*We are referring Bloom Taxonomy of action verbs

•http://www.clemson.edu/assessment/assessmentpractices/referencematerials/documents/Blooms%20Taxonomy%20Action%20Verbs.pdf

Operating Systems

- Outline
  - Computer System Structure
  - Operating System Structure
  - System Processes
  - Threads
    - ULT & KLT
    - Pthreads & cloning processes
    - Threading for improving performance on Multicore Architectures
    - create their own ULT Library
  - CPU Scheduling
    - Scheduling for SMP/Multicore Architectures
  - Synchronization & Concurrency
    - Race Conditions, Deadlocks
    - IPC Mechanisms
  - Memory Management
  - I/O Management
  - File Systems

*Apply** 24 hrs

*Knowledge** 8 hrs

*Apply** 32 hrs

Total 128 hrs

64 hrs/128 = 50%

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Distributed Systems

- Recently changed to: Parallel Programming & Distributed Systems
- Outline
  - Parallel Programming Concepts
  - Tools for Parallel Programming
    - Compilers, Parallel Studio
  - Windows Threads
  - Parallel Programming Models & Design
  - OpenMP
  - MPI (Clusters Programming)
  - Distributed Systems Introduction
  - Sockets Programming
    - TCP/UDP
  - Client/Server & P2P Applications
  - Distributed Systems Synchronization Algorithms
  - Atomic Transactions
  - RPCs
  - RMIs
  - Corba
  - Web Services

*Apply**

64 hrs

Total 128 hrs

64 hrs/128 = 50%

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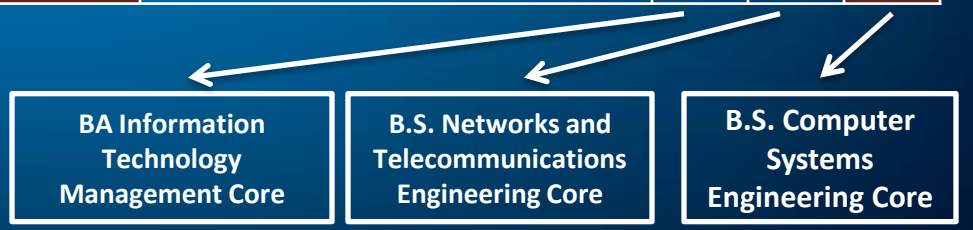
Learning Outcomes (1/2)

Operating Platforms	Operating Systems	Distributed Systems	Bachelor Programs		
Describe HT & MC like logical & physical CPUs			BA IT	BS N&T	
Understand the benefit of MC in multiprogramming environments	Understand the benefit of MC in multiprogramming environments		BA IT	BS N&T	BS CSE
Measure the difference of HT & MC	Measure the difference of HT & MC		BA IT	Bcs N&T	BS CSE
	Describe how threads are implemented in an OS				BS CSE
	OS Scheduling for SMP & Multicore				BS CSE
Problem decomposition in tasks		Problem decomposition in tasks	BA IT	BS N&T	BS CSE
	User Level Threads & Kernel Level Threads				BS CSE



*Knowledge** *Apply**

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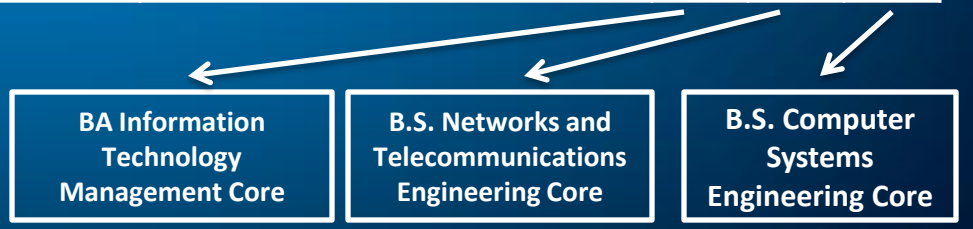
Learning Outcomes (2/2)

Operating Platforms	Operating Systems	Distributed Systems	Bachelor Programs		
	Threading with OS Threads (Clone)				
Threading with OS Threads (Windows)	Threading with Posix Library (Pthreads)	Threading with OS Threads (Windows)			
Race conditions and Deadlocks	Race conditions and Deadlocks	Race conditions and Deadlocks	**BA IT**	**Bcs N&T**	**BS CSE**
	How IPCs are implemented				**BS CSE**
Using tools for performance and correctness		Using tools for performance and correctness	**BA IT**	**BS N&T**	**BS CSE**
	Use of IPCs for process & threads synchronization				**BS CSE**
		Parallel Applications in Shared Memory vs. Non Shared memory		**BS N&T**	**BS CSE**



*Knowledge** *Apply**

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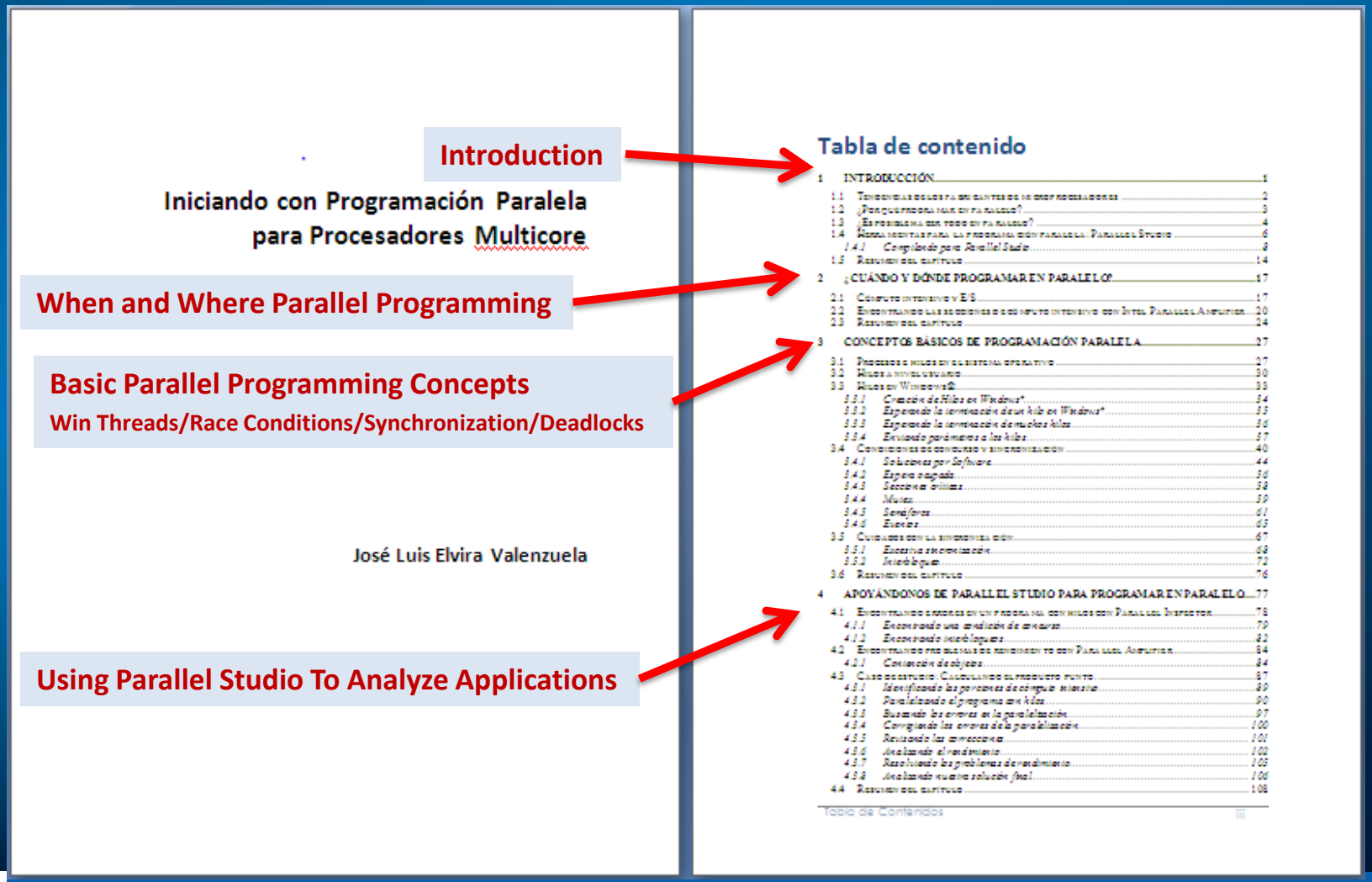
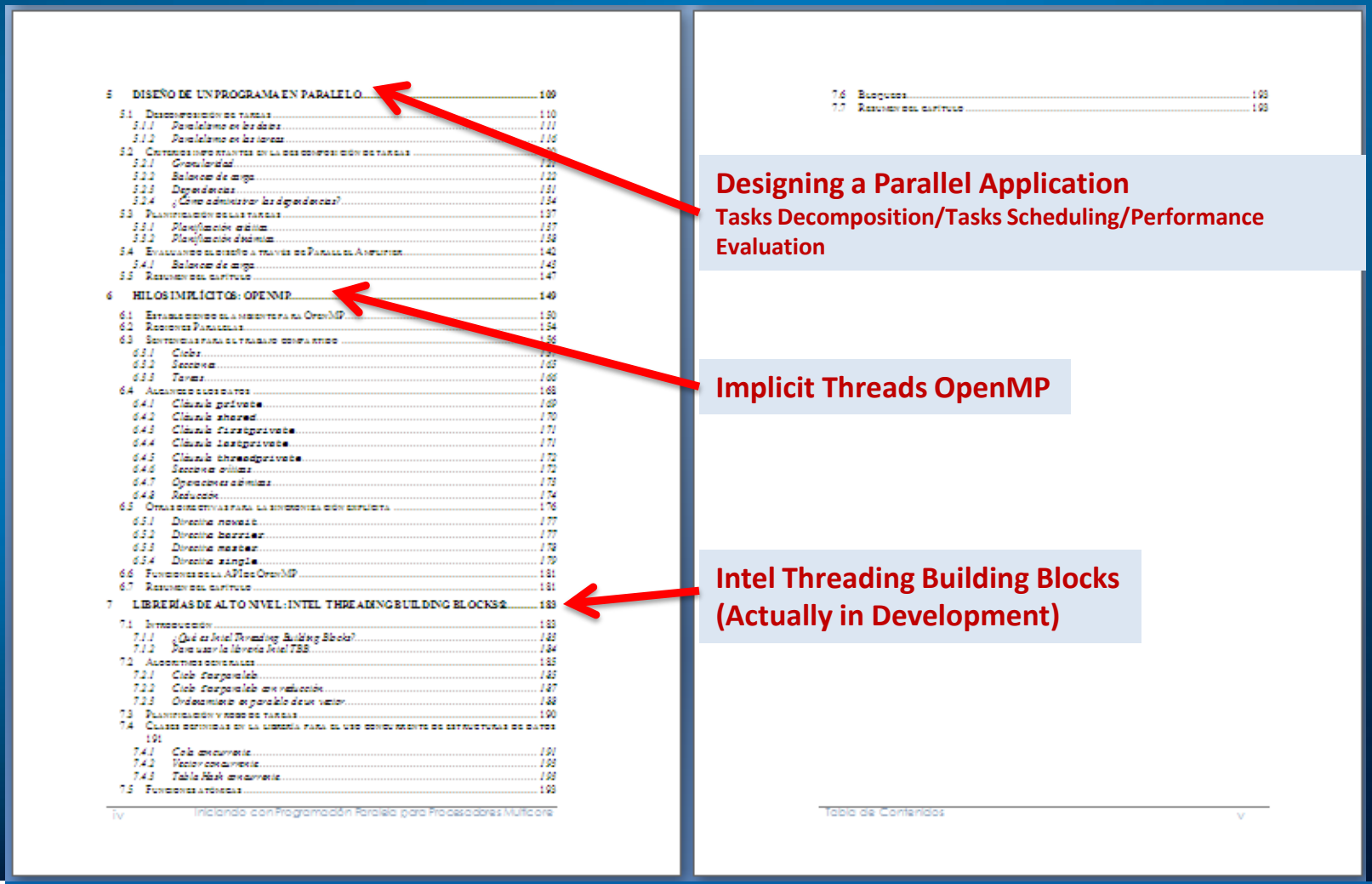
Notes developed included in our courses (In Spanish) (1/2)



Notes developed included in our courses (In Spanish) (2/2)



Designing a Parallel Application
Tasks Decomposition/Tasks Scheduling/Performance Evaluation

Implicit Threads OpenMP

Intel Threading Building Blocks (Actually in Development)

Intel Challenge

- Multicore programming contest called “ITESO-Intel Challenge”.
- Intel as a sponsor of the competition
- Since Autumn 2006, Intel Challenge has been realized 6 times at ITESO
- Within ACM programming contest
- In the challenge, participants has to optimize a CPU intensive program to run in Multicore architecture.

- Open to undergraduate students of all universities in Guadalajara and Mexico.
- Las edition also included a new version of this contest aimed at high school student with Two-folded intention:
  - Introduce high school students to Multicore programming
  - Develop an interest to become IT professionals.

- The contest aims to disseminate:
  - What Multicore means
  - Why parallel programming to achieve maximum performance
  - Software industry challenges
  - How to thread an application
  - Using tools for correctness and maximize performance

Faculty Training

- ITESO has collaborated with Intel Education in Faculty Training for to participate teaching Multi-Core programming to universities in México and Latin America.
  - Created the Spanish version of the Multi-core Programming for Academia Module
  - Since 2007 course has been replicated 10 times to professors of more than 50 universities
    - http://software.intel.com/en-us/articles/iac-recognition

Professional Applications Projects

- ITESO has defined a program called Professional Application Projects (PAP)
- Students involved in a real-world industrial project
  - Over a period ranging from eight to twelve months.
  - Two consecutive school terms in order to obtain their degree.
- Since 2009, there have been PAPs related to Multicore Programming
- Involving collaboration of industrial partners
- Participated in the development of a traffic simulator
  - Particularly optimizing code to perform calculations using Multicore architectures.